

WHAT IS CLAIMED IS:

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1. A semiconductor device, exchanging a data series with an exterior of the device, comprising:

10 a register which stores a first data item
of said data series, the first data item immediately
preceding a second data item of said data series;
and

an exchange circuit which exchanges with the exterior of the device a signal indicative of which bit or bits of the first data item are to be inverted to convert the first data item into the second data item, the exchanging of the signal effectively achieving the exchanging of the data series.

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2. The semiconductor device as claimed in
25 claim 1, wherein said exchange circuit generates the
second data item in response to the signal received
from an exterior of the device, and sends the second
data item to an internal circuit of the device.

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35 3. The semiconductor device as claimed in
claim 1, wherein said exchange circuit generates the
signal in response to the second data item received
from an internal circuit of the device, and sends
the signal to an exterior of the device.

5 4. The semiconductor device as claimed in
claim 1, wherein said exchange circuit replaces said
first data item stored in said register with said
second data item.

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15 5. The semiconductor device as claimed in
claim 2, wherein said exchange circuit stores said
first data item in said register when the first data
item is received, and generates said second data
item when said signal is received.

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25 6. The semiconductor device as claimed in
claim 3, wherein said exchange circuit stores said
first data item in said register when said first
data item is received, and generates said signal
when said second data item is received.

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7. The semiconductor device as claimed in
claim 1, wherein said register is reset in response
to a reset signal.

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8. The semiconductor device as claimed in
claim 1, wherein said semiconductor device further
comprises a memory array, and said register is reset
in response to a refresh command received from an
5 exterior of the device.

10 9. The semiconductor device as claimed in
claim 1, wherein said signal is a pulse.

15 10. The semiconductor device as claimed
in claim 2, wherein said exchange circuit includes a
data input unit which latches said signal, and said
semiconductor device further comprises a circuit
20 which receives a chip select signal from an exterior
of the device, and said data input unit latches said
signal in response to said chip select signal.

25 11. The semiconductor device as claimed in
claim 10, wherein said signal is a pulse, and said
data input unit latches said signal in response to
30 an edge of the pulse.

35 12. The semiconductor device as claimed in
claim 1, wherein said exchange circuit includes a
data input unit which latches said signal, and said

semiconductor device further comprises a clock generation unit which generates an internal clock in response to a clock received from an exterior of the device, and said data input unit latches said signal
5 in synchronism with the internal clock.

10 13. The semiconductor device as claimed in claim 1, wherein said exchange circuit includes a data input unit which latches said signal, and said semiconductor device further comprises a clock generation unit which generates an internal clock in response to a clock input from an exterior of the device, and said data input unit latches said signal,
15 which is a pulse, in response to an pulse edge of said signal during a predetermined period defined relative to said internal clock.

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25 14. The semiconductor device as claimed in claim 3, wherein said semiconductor device is a controller which controls a semiconductor memory device, and resets said register in relation to a refresh command when issuing the refresh command to said semiconductor memory device.

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35 15. The semiconductor device as claimed in claim 1, wherein said semiconductor device further comprises an interface which selectively provides a connection with a plurality of semiconductor devices,

and said register is provided for each of said plurality of semiconductor devices.

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16. The semiconductor device as claimed in
claim 2, wherein said exchange circuit generates
said second data item by performing an Exclusive-Or
10 operation of said first data item and said signal.

15 17. The semiconductor device as claimed in
claim 3, wherein said exchange circuit generates
said signal by performing an Exclusive-Or operation
of said first data item and said second data item.

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18. A system comprises the semiconductor
devices claimed in claim 1, wherein registers of
25 said semiconductor devices store a common first
information.

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19. A method for exchanging a data series
with an exterior of the device, comprising:
a step of storing a first data item of
said data series, the first data item immediately
35 preceding a second data item of said data series;
and

a step of exchanging with the exterior of

the device a signal indicative of which bit or bits
of the first data item are to be inverted to convert
the first data item into the second data item, the
exchanging of the signal effectively achieving the
5 exchanging of the data series.

10 20. The method as claimed in claim 19,
wherein said second data item is generated by
performing a logical operation between a signal
received from an exterior of the device and said
first data item in said register.

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20 21. The method as claimed in claim 19,
wherein said signal is generated by performing a
logical operation between a second data item
received from an exterior of the device and said
first data item in said register.

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30 22. The method of information processing
as claimed in claim 18, wherein the method further
comprises a step of replacing said first information
stored in said register with said second information.

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